REMARKS

Reconsideration of the above-identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1-10, 20 and 26 are pending in this application. By this Amendment, Applicants have amended Claims 1 and 20, and added new Claim 26. Claim 21 was withdrawn. The claim amendments were made to more precisely define the invention in accordance with 35 U.S.C. 112, paragraph 2. These amendments have not been necessitated by the need to distinguish the present invention from any prior art. It is respectfully submitted that no new matter has been introduced by these amendments, as support therefor is found throughout the specification and drawings. For example without limitation, support for the amendments to the Claims can be found at page 10, 3rd-5th paragraphs and the associated Figures 3 and 4 among other places.

In the Office Action, Claims 1-4, 7, 8 and 20 were rejected under 35 U.S.C. §102(b) over Japanese patent application no. 2001-351995 to Shigenobu et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

Shigenobu et al. disclose a semiconductor with a high-voltage circuit section separated by the isolation insulator layer 45 with the memory cell array section. A low-battery section is separated by the isolation insulator layer 45 with memory cell array section is shown in Figure 36 and described in paragraphs 104-106. Memory cell transistors are divided by an isolation insulators layer 5. The high-voltage transistors, which adjoin mutually, are separated by the isolation insulator layer 5. In other words and as clearly shown in Figure 36, the memory cell has transistors with wells 47 on one

side and different wells 5 on the other. Further, as the Examiner notes in the Office Action, first and second transistors, separated by the wells 5, are between the wells 47. In contrast, Claim 1 recites, *inter alia*, a semiconductor device including a first high breakdown voltage transistor formed in the first semiconductor layer, a second high breakdown voltage transistor formed in the second semiconductor layer, and a first isolation region formed between the first semiconductor layer and the second semiconductor layer, the first isolation region surrounding the first and second high breakdown voltage transistors individually and having a depth that reaches the insulating layer. Consequently, each of the first and second high breakdown voltage transistors are individually surrounded by the isolation layer. Shigenobu et al. do not disclose or suggest such a structural configuration because its isolation region 47 surrounds a plurality of high voltage transistors. Accordingly, Claim 1 and each of the claims depending therefrom distinguish the subject invention from Shigenobu et al. and an action acknowledging the same is respectfully requested.

With respect to Claim 20, Shigenobu et al. only show memory cells having transistors with wells 47 without an oxide film as noted above. However, Claim 20 recites a semiconductor device including a support substrate, an insulating layer formed on the support substrate, a high breakdown voltage transistor, a low breakdown voltage transistor, wherein the high breakdown voltage transistor is within a first isolation region having a depth that reaches the insulating layer such that the first isolation region isolates the high breakdown voltage transistor from other transistors, and the low breakdown voltage transistor is adjacent to a second isolation region having a depth that does not reach the insulating layer. Shigenobu et al. do not disclose or suggest such a structural configuration but rather shows multiple transistors surrounded by the

isolation layer. Thus, Claim 20 distinguishes the subject invention from Shigenobu et al. and an action acknowledging the same is respectfully requested.

In the Office Action, Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) over Shigenobu et al. in view of U.S. patent application no. 2004/0079993 to Ning et al.

It is respectfully submitted that Ning et al. do not overcome the deficiencies of Shigenobu et al., as noted above with respect to Claim 1. In particular, neither Shigenobu et al. nor Ning et al. disclose or suggest, either alone or in combination, in whole or in part, a semiconductor device including, *inter alia,* first isolation region surrounding the first and second high breakdown voltage transistors individually and having a depth that reaches the insulating layer as recited in Claim 1. Accordingly, Claims 5 and 6, by virtue of their dependence on Claim 1, are not rendered obvious by the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

In the Office Action, Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) over Shigenobu et al. in view of U.S. Patent No. 5,965,921 to Kojima.

It is respectfully submitted that Kojima does not overcome the deficiencies of Shigenobu et al., as noted above with respect to Claim 1. In particular, neither Shigenobu et al. nor Kojima disclose or suggest, either alone or in combination, in whole or in part, a semiconductor device including, *inter alia,* first isolation region surrounding the first and second high breakdown voltage transistors individually and having a depth that reaches the insulating layer as recited in Claim 1. Accordingly, Claims 9 and 10, by virtue of their dependence on Claim 1, are not rendered obvious

by the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

Applicant has added new Claim 26 which is directed to additional patentable aspects of the subject invention. Applicant respectfully submits that new Claim 26 patentably distinguishes over the art of record, and allowance of this claims is respectfully requested.

Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105. It is respectfully submitted that all of the claims now remaining in this application are in condition for allowance, and such action is earnestly solicited.

If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

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Respectfully submitted,

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